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The major accomplishments (in chronological order) of this quarter include:

- Definition of five level hierarchy
- Linear array representation of processor
- Node/Network partitioning
- Primitive definitions for distributed execution
- Definition of a mechanism to allow recursion

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OPTICAL SYMBOLIC PROCESSOR FOR EXPERT SYSTEM EXECUTION

Quarterly R&D Status Report No. 3

For the period from 1 December 1986 to 28 February 1987

Approved for public release; distribution unlimited.

ARPA Order 5794
Program Code 6D10
Period of Performance: 1 June 1986 to 31 May 1987
Amount of Contract: $357,385
Contract Number: F49620-86-C-0082

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Air Force Office of Scientific Research

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Department Manager

INTRODUCTION

The goal of this program is to develop a concept for an optical computer architecture for symbolic computing by defining a computation model of a high level computer language, examining the possible devices for the ultimate construction of a processor, and by defining required optical operations.

PROGRESS FOR THE PERIOD

In this quarter we have developed the portions of an optical computer architecture which performs the graph manipulations required for combinator graph reduction (CGR). This was achieved through the use of a heirarchical design processes. Five levels of complexity were defined between hardware and the algorithms for CGR. The architecture was developed by employing the assessments of optical architectures made in previous quarters to define the potential operations which could be performed with optical components. These operations and the definition of the primitive operations required to execute each combinator where then used to develop a framework architecture which has the potential to perform CGR.

The major accomplishments (in chronological order) of this quarter include:

Definition of Five level heirarchy

Five levels of complexity where defined which allow complexity to be compartmentalized. This heirarchy is much like those used in electronic systems so that the operation of the computer does not have to be designed at the transistor level.

Linear Array representation of processor

Since close to 1000 bits of data will be required to store that data needed to represent a node in graph form, a 1000 x 1000 array of optical gates can be formated as a linear array of processors. This has the advantage that data movements in the plane can be regularized and interconnections simplified.

Node/Network partitioning

Each node in the linear represtion was partioned into a processor and a "network" part. The processor part performs the computation, while the network part moves data amoung the nodes.

Primitive definitions for distributed execution

Distributed algorithms were developed for the combinators which could execute on the array of processors.

Recursion

Algorithms to allow recursion where developed for the processor. These algorithms allow the processor, which has no location addressable memory or stack, recursively execute functions by allocating nodes and copying portions of the graph while combinator reduction is occuring in parallel.

In the next quarter we will be examing how primitive functions (such as plus, or, compare) can be performed by this architecture. We will also be investigating how this processor can be best integrated with the knowledge base of an expert system.

Simulations of the optical deflector have shown that the easily saturated nonlinearity of GaAs may not be suitable for constructing the nonlinear prism deflector. In the next quarter we will be evaluating GaAs properties, as well as other materials to see if enough deflection can be obtained for the device to be useful.

EXPERIMENTAL OR SPECIAL EQUIPMENT PURCHASED OR CONSTRUCTED

None.

CHANGE IN KEY PERSONNEL

There were no changes in key personnel during this reporting period.

INFORMATION DERIVED FROM MEETINGS, VISITS, BRIEFINGS, AND SCIENTIFIC PAPERS

Because the majority of the work in this quarter was definition of operations and functions, little outside information employed other than those sources referenced previously.

General information pertaining to optical computing was obtained at the DARPA/AFOSR Optics program review in Leesburg, VA in February.

PROBLEMS NEEDING GOVERNMENT ASSISTANCE

None.

DEVIATIONS FROM THE PLANNED EFFORT

We have not been able to fully examine the device for reconfigurable interconnects. More progress on the device portion of this program should begin next quarter.

UNITED STATES AIR FORCE QUARTERLY CONTRACTOR R & D STATUS REPORT	REPORT FOR QUARTER ENDING. FEB 1987
OPTICAL SYMBOLIC PROCESSOR FOR EXPERT SYSTEM EXECUTION	INITIAL CONTRACT PHASE

TO:	U.S.A.F., A.F.S.C. Air Force Office of Scientific Research Building 410 Bolling AFB, DC 20332-6448	FROM:	HONEYWELL, INC. PSC 10701 LYNDALE AVE. SO. BLOOMINGTON, MN. 55420

1. Description Of Contract	a. Type : Cost Plus Fixed Fee	b. Contract Number :	F49620-86-C-0082
	c. Contract Value : $357,385		

2. EXPENDITURES		3. COMMITMENTS	
a. Costs	b. Fee	a. Materials	b. Subcontracts
$144,493	$0	$0	$18,800

4. Funding Limitation	5. Estimated Date of Completion	6. Estimated Funds to Complete
$357,385	MAY 31, 1987	$357,385